Please amend the specification as follows:

Page 14, paragraph beginning at line 9, please delete in its entirety and insert therefor the following new paragraph:

An image system according to the present invention is characterized by comprising an optical system for receiving an optical image from an object and guiding the optical image to a predetermined position; image processing means including a sensor for photoelectrically converting the optical image guided to the predetermined position into an electrical signal corresponding to a light amount of the optical image in units of pixels; and a signal processing device for processing an output from the image processing means in a predetermined form, and outputting the output, the sensor comprising a photoelectric conversion element placed at the predetermined position, an output circuit including an amplification MOS transistor connected to the photoelectric conversion element serving to amplify and output an output from the photoelectric conversion element at a first timing and output noise independent of the output from the photoelectric conversion element at a second timing, and a noise reduction circuit connected to an output of the output circuit, having the same impedance at the first and second timings when viewed from the output circuit, and serving to obtain a difference between outputs from the output circuit at the first and second timings.

Page 15, paragraph beginning at line 6, please delete in its entirety and insert therefor the following new paragraph:

Another image system according to the present invention is characterized by comprising an optical system for receiving an optical image from an object and guiding the optical image to a predetermined position; image processing means including a sensor for photoelectrically converting the optical image guided to the predetermined position into an electrical signal corresponding to a light amount of the optical image in units of pixels; and a

signal processing device for processing an output from the image processing means in a predetermined form, and outputting the output, the sensor comprising a photoelectric conversion element placed at the predetermined position, an output circuit including an amplification MOS transistor connected to the photoelectric conversion element serving to amplify and output an output from the photoelectric conversion element at a first timing and output noise independent of the output from the photoelectric conversion element at a second timing, a signal line connected to the output circuit; and a noise reduction circuit including a clamp capacitor having one end connected to the signal line, a sample/hold capacitor connected between the other end of the clamp capacitor and a predetermined potential, and an impedance correction circuit for selectively applying a capacitance less than a capacitance two times a series capacitance of the clamp capacitor and the sample/hold capacitor between the signal line and the predetermined potential, and serving to obtain a difference between outputs from the output circuit at the first and second timings.

Page 16, paragraph beginning at line 9, please delete in its entirety and insert therefor the following new paragraph:

A still another image system according to the present invention is characterized by comprising an optical system for receiving an optical image from an object and guiding the optical image to a predetermined position; image processing means including a sensor for photoelectrically converting the optical image guided to the predetermined position into an electrical signal corresponding to a light amount of the optical image in units of pixels; and a signal processing device for processing an output from the image processing means in a predetermined form, and outputting the output, the sensor comprising a photoelectric conversion element placed at the predetermined position, an output circuit including an amplification MOS transistor connected to the photoelectric conversion element and serving to amplify and output an output from the photoelectric conversion element at a first timing

and output noise independent of the output from the photoelectric conversion element at a second timing, a signal line connected to an output of the output circuit, a source follower circuit having an input connected to the signal line, a clamp capacitor having one end connected to an output of the source follower circuit, a sample/hold capacitor connected between the other end of the clamp capacitor and a first predetermined potential, and a clamp transistor connected between the other end of the clamp capacitor and a second predetermined potential and serving to selectively clamp the sample/hold capacitor.

Page 17, paragraph beginning at line 11, please delete in its entirety and insert therefor the following new paragraph:

A still further image system according to the present invention is characterized by comprising an optical system for receiving an optical image from an object and guiding the optical image to a predetermined position; image processing means including a sensor for photoelectrically converting the optical image guided to the predetermined position into an electrical signal corresponding to a light amount of the optical image in units of pixels; and a signal processing device for processing an output from the image processing means in a predetermined form, and outputting the output, the sensor comprising a photoelectric conversion element placed at the predetermined position, an output circuit including an amplification MOS transistor connected to the photoelectric conversion element and serving to amplify and output an output from the photoelectric conversion element at a first timing and output noise independent of the output from the photoelectric conversion element at a second timing, a signal line connected to an output of the output circuit, a clamp capacitor having one end connected to the signal line, a sample/hold capacitor connected between the other end of the clamp capacitor and a first predetermined potential, and a clamp transistor connected between the other end of the clamp capacitor and a second predetermined potential and serving to clamp the sample/hold capacitor at a predetermined timing.

Page 26, paragraph beginning at line 14, please delete in its entirety and insert therefor the following new paragraph:

A solid-state imaging device according to the present invention is characterized by comprising a photoelectric conversion element; an output circuit including an amplification MOS transistor connected to the photoelectric conversion element and serving to amplify an output from the photoelectric conversion element at a first timing and output noise independent of the output from the photoelectric conversion element at a second timing; and a noise reduction circuit connected to an output of the output circuit, having the same impedance at the first and second timings when viewed from the output circuit, and serving to obtain a difference between outputs from the output circuit at the first and second timings.

Page 28, paragraph beginning at line 24, please delete in its entirety and insert therefor the following new paragraph:

A solid-state imaging device according to the present invention is characterized by comprising: a photoelectric conversion element; an output circuit including an amplification MOS transistor connected to the photoelectric conversion element and serving to amplify an output from the photoelectric conversion element at a first timing and output noise independent of the output from the photoelectric conversion element at a second timing; a signal line connected to the output circuit; and an impedance correction circuit including a clamp capacitor having one end connected to the signal line, a sample/hold capacitor connected between the other end of the clamp capacitor and a predetermined potential, and an impedance correction circuit for selectively applying a capacitance less than two times a difference between a series capacitance of the clamp capacitor and the sample/hold capacitor and the clamp capacitor between the signal line and a predetermined potential, and serving to obtain a difference between outputs from the output circuit at the first and second timings.

Page 30, paragraph beginning at line 14, please delete in its entirety and insert

therefor the following new paragraph:

A solid-state imaging device according to the present invention is characterized by comprising: a photoelectric conversion element; an output circuit including an amplification MOS transistor connected to the photoelectric conversion element and serving to amplify an output from the photoelectric conversion element at a first timing and output noise independent of the output from the photoelectric conversion element at a second timing; a signal line connected to an output of the output circuit; a clamp capacitor having one end connected to the signal line; a sample/hold capacitor connected between the other end of the clamp capacitor and a first predetermined potential; and a clamp transistor connected between the other end of the clamp capacitor and a second predetermined potential and serving to clamp the sample/hold capacitor at a predetermined timing.

Page 63, paragraph beginning at line 19, please delete in its entirety and insert therefor the following new paragraph:

FIG. 5 shows an embodiment of a video camera using the MOS sensor according to the present invention. As shown in FIG. 5, a video camera according to the present invention comprises a lens 101 for picking up an image of an object, a focus adjusting mechanism 102 for adjusting the focus of the optical system, a diaphragm/focus adjusting circuit 103 for controlling a diaphragm mechanism 116 and the focus adjusting mechanism 102, an MOS sensor 105 for converting an optical image formed by the lens 101 into an electric signal corresponding to the quantity of light of the optical image in pixel units, a color filter array 104 disposed on the image forming side of the MOS sensor 105 and having a color filer section for each pixel for any one of R, G and B, a current-to-voltage converter 106 for converting the electric signal obtained by the MOS sensor 105 into a voltage signal, an AGC circuit 107 for adjusting the level of the voltage signal obtained through the current-to-voltage converter 106, a clamp (CLP) circuit 108 for clamping voltage signals having levels

aligned by the AGC circuit 107, an analog-to-digital converter (ADC) 109 for converting an output from the CLP circuit 108 into a digital signal having the corresponding level, a timing control circuit 110 for generating a timing pulse (a clock signal) for arranging timing which is the base of the operation of the system, a TG/SG circuit 111 for controlling the operation of the MOS sensor 105 in synchronization with the clock signal output from the timing control circuit 110, a process control circuit 112 for processing a digital signal output from the ADC circuit 109, an encoder circuit 113 for encoding a signal processed by the process control circuit 112, an output circuit 114 for outputting an encoded signal and a digital-to-analog converter 115 for converting a signal output through output circuit 114 into an analog signal.

Page 69, paragraph beginning at line 10, please delete in its entirety and insert therefor the following new paragraph:

FIG. 7 shows another embodiment of the video camera comprising the MOS sensor according to the present invention. The video camera shown in FIG. 7 has a three-plate type structure, in which the imaging system is divided into three (RGB: Red, Green and Blue) systems as compared with the structure shown in FIG. 5 which has the single-plate type imaging system. As shown in FIG. 7, a video camera according to the present invention comprises a lens 101 which is an optical system for forming an image of an object, a focus adjusting mechanism 102 for adjusting the focus of the optical system, a diaphragm/focus adjusting circuit 103 for controlling a diaphragm mechanism 116 for adjusting the quantity of incidental light into the optical system and a focus adjusting mechanism 102, a color separating prisms 201R, 201G and 201B for separating the optical image formed by the lens 101 into three primary color components (RGB), MOS sensors 105R, 105G and 105B for the R component, the G component and the B component which are imaging devices on which the image separated into the three primary color components R, G and B by the color

separating prisms 201R, 201G and 201B is formed and in which the image is converted into an electric signal corresponding to the quantity of light of the optical image in pixel units, current-to-voltage converters 106R, 106G and 106B for the R component, the G component and B component for converting the electric signals obtained by the MOS sensors 105R, 105G and 105B into voltage signals, AGC circuits 107R, 107G and 107B for the R component, the G component and the B component for adjusting the levels of the voltage signals obtained by the current-to-voltage converters 106R, 106G and 106B, clamp (CLP) circuits 108R, 108G and 108B for the R component, the G component and the B component for clamping the voltage signals having the levels aligned by the AGC circuits 107R, 107G and 107B, analog-to-digital converters (ADC) 109R, 109G and 109B for the R component, the G component and the B component for converting outputs from the CLP circuits 108R, 108G and 108B into digital signal having the corresponding levels, a timing control circuit 110 for generating timing pulses for arranging the timing which is the base of the operation of the system, a TG/SG circuit 111 for the R component, the G component and the B component for controlling the operation of the MOS sensor 105 in synchronization with the timing pulse output from the timing control circuit 110, a process control circuit 112 for processing digital signals from the ADC circuits 109R, 109G and 109B, an encoder circuit 113 for encoding the signal processed by the process control circuit 112, an output circuit 114 for controlling input and output of the encoded signal and a digital-to-analog converter 115 for converting the signal through the output circuit 114 into an analog signal.

Page 73, paragraph beginning at line 20, please delete in its entirety and insert therefor the following new paragraph:

According to this embodiment, a video camera having a necessity of processing an image at 30 frames in one second and capable of reducing electric power consumption, lowering the required voltage level can be provided which is enabled to cancel a fixed pattern

noise component in a horizontal blanking period and obtain an image signal exhibiting excellent S/N and an excellent quality of the formed image.

Page 74, paragraph beginning at line 1, please delete in its entirety and insert therefor the following new paragraph:

Although the above-mentioned structures are arranged to use the color separating prism to separate the optical image into the three primary color components R, G and B, a diachronic mirror may be employed to separate the optical image. In this case, diachronic mirrors for reflecting red, green and blue components are employed to separate and distribute incidental light so as to separate the optical image into the R, G and B components. The optical images are formed by MOS sensors for R, G and B images so that R, G and B image signals are obtained. Thus, a structure can be formed in which any prism is required to separate the optical image into three primary color components.

Page 80, paragraph beginning at line 7, please delete in its entirety and insert therefor the following new paragraph:

This embodiment enables the electric power consumption to be reduced, the required voltage level to be lowered and a high speed successive image picking-up to be performed with a high S/N ratio such that a plurality of frames can successively be picked up in one second. Thus, a still camera exhibiting a compact size, excellent function and satisfactory performed can be obtained. That is, a still camera can be provided which is capable of canceling fixed pattern noise component, which is a problem for the MOS sensor, in a short time, which exhibits excellent S/N and which enables a high quality picture to be obtained.

Page 84, paragraph beginning at line 5, please delete in its entirety and insert therefor the following new paragraph:

An MOS sensor 608 is disposed at the imaging position of the lens 60. The MOS sensor 608 is a linear sensor having light receiving sections (photodiodes) corresponding to

pixels and disposed in one-dimensional configuration, the MOS sensor 608 being a monochrome solid-state imaging device having the noise canceler circuit according to the present invention.

Page 85, paragraph beginning at line 15, please delete in its entirety and insert therefor the following new paragraph:

The polygonal mirror 612 is controlled by the system controller 610 so that the surface of the cylindrical photosensitive drum 613 is scanned with the spot-shaped laser beam corresponding to the output speed of the signal output from the MOS sensor 608. Assuming that the direction of rotation of the photosensitive drum 613 is the main scanning direction, the laser beam is scanned in a direction perpendicular to the rotation direction, the surface of the photosensitive drum 613 loses the electric charges to correspond to the quantity of the laser beam. Thus, a latent image corresponding to the image of the original document is formed on the surface of the photosensitive drum 613. When the photosensitive drum 613, at a position downstream of the image forming position, passes through the position of a developing section 614 for converting the latent image into a visible image, the latent image at the corresponding position is converted into a visible image with toner supplied from the developing section 614. The toner image is transferred to copy paper sheets sequentially picked up from an accommodating tray 615 for the copy paper sheets and conveyed to a conveying passage 616 below the photosensitive drum 613.

Page 92, paragraph beginning at line 9, please delete in its entirety and insert therefor the following new paragraph:

In the handy image scanner shown in FIG. 12, the frame 701 is placed on an original document. Then, it is manually slid on the original document to scan the original document. At this time, a roller 704 is disposed to synchronize detection of the line position and the reading timing in order to output the image of the original document for line units through

the slit 701a.

Page 93, paragraph beginning at line 21, please delete in its entirety and insert therefor the following new paragraph:

The signal read from the MOS sensor 706 is subjected to position correspondence in accordance with an output from the encoder 705 so as to be used to control the reading timing.

Page 94, paragraph beginning at line 12, please delete in its entirety and insert therefor the following new paragraph:

As described above, the handy image scanner according to this embodiment is arranged such that the frame 701 is placed on the original document and then manually moved on the surface of the original document. To output the image of the original document in unit of lines through the slit 701[a], the roller 704 is provided which synchronizes the detection of the position of the line and the reading timing. The roller 704 is brought into contact with the original document so as to be rotated because of the friction with the original document. As a result, a detection signal representing the direction and amount of rotation of the roller 704 is output from the encoder 705. In response to the detection signal supplied from the encoder 705, a control means (not shown) performs control in such a manner that the output signal from the MOS sensor 706 coincides with each line.

Page 103, paragraph beginning at line 24, please delete in its entirety and insert therefor the following new paragraph:

Generally, in an amplification-type MOS-type solid-state imaging device, an output signal from the photodiode which is a light receiving element corresponding to a pixel is amplified by an amplification transistor provided in the same unit cell. During amplification, a variation of the threshold voltage of the amplification transistors is superposed on the

signal. Therefore, even if the potentials of the photodiodes in each unit cell are the same, the output signals may vary since the amplification transistors are different for the cells and the threshold voltages are also different for the cells. Therefore, when an image picked-up by the amplification-type MOS-type solid-state imaging device is reproduced, noise due to the threshold variation of the amplification transistor are generated.

A16 cancel

Page 104, paragraph beginning at line 13, please delete in its entirety and insert therefor the following new paragraph:

As described above, in an amplification-type MOS-type solid-state imaging device, the threshold voltages of the amplification transistors in the unit cells are different from each other and the threshold voltage is unique to the unit cell. Therefore, it is unavoidable to generate noise fixedly distributed on the reproduced image, i.e., a two-dimensional noise. Since this noise is fixed in the position on the image, it is called a fixed pattern noise.

Page 105, paragraph beginning at line 4, please delete in its entirety and insert therefor the following new paragraph:

FIG. 17 shows the arrangement of an MOS-type solid-state imaging device according to a twelfth embodiment of the present invention. Unit cells P4-i-j are arranged in the form of a two-dimensional matrix. Although FIG. 17 shows only a 2 x 2 matrix, the actual apparatus has several thousand cells x several thousand cells. Reference symbol denotes a variable in the horizontal (row) direction; and, a variable in the vertical (column) direction. The details of the unit cell P4-i-j are shown in FIG. 21.

A17

Page 106, paragraph beginning at line 15, please delete in its entirety and insert therefor the following new paragraph:

Connection points between the MOS transistors 26-1, 26-2, ... and 28-1, 28-2, ... are connected to one ends of clamp capacitors 32-1, 32-2, ... through sample/hold transistors 300-1, 30-2, ... Sample/hold capacitors 34-1, 34-2, ... and clamp transistors 40-1, 40-2, ...

A18 cont

are connected in parallel to the other ends of the clamp capacitors 32-1, 32-2, ... The other ends of the sample/hold transistors 30-1, 30-2, ... are grounded. The other ends of the clamp capacitors 32-1, 32-2, ... are connected to a signal output terminal (horizontal signal line) 15 through a horizontal selection transistors 12-1, 12-2, ...

Page 108, paragraph beginning at line 13, please delete in its entirety and insert therefor the following new paragraph:

In general, in the amplification-type MOS-type solid-state imaging device, since variations in the threshold voltages of the amplification transistors 64 are superimposed on signals, even if the potentials of the photodiodes 62 are the same, the output signals vary. When a picked-up image is reproduced, therefore, two-dimensional noise (called fixed pattern noise because the noise is fixed to a specific place) corresponding to the threshold variations of the amplification transistors 64 is generated. Even if the light receiving portion is uniformly irradiated with light, the output signals from the pixels are different. Noise distributed two-dimensionally in the image is fixed with respect to the position of the pixels and is called a fixed pattern noise.

Page 119, paragraph beginning at line 27, please delete in its entirety and insert therefor the following new paragraph:

Since the impurity concentration of an n-type photodiode 90 can be arbitrarily set to a certain degree, not many limitations are imposed in terms of manufacture. With the above impurity concentrations, the sheet resistance of the p^+-type well 86 is about 100 k $\Omega/\square$. As described above, with such a large value, the noise caused in the CCD is very small.

Page 120, paragraph beginning at line 14, please delete in its entirety and insert therefor the following new paragraph:

According to the NTSC scheme, which is the existing television scheme, the noise reduction circuit is operated in an interval of about 11 [μs], which is a horizontal blanking

interval. Disturbances in the potential of the p-type well 86 must be suppressed to about 0.1 (mV) within this interval.

Page 120, paragraph beginning at line 20, please delete in its entirety and insert therefor the following new paragraph:

Such a small value as 0.1 (mV) is set because the noise voltage output of the CCD corresponds to this. According to a detailed analysis, to settle the disturbances to a value as small as 0.1 (mV) within the very short time interval of 11 [μ s], the sheet resistance of the p^+-type well 86 must be set to 1 kΩ/□ or less. This is a bout 1/100 the sheet resistance of the conventional CCD.

Page 121, paragraph beginning at line 1, please delete in its entirety and insert therefor the following new paragraph:

For this purpose, the impurity concentration of the p^+-type well 86 must be increased to about 100 times. Such a concentration cannot be set in the CCD, as described above with reference to the p-type substrate. Furthermore, in the high-vision television scheme, the horizontal blanking interval is 3.77 (μ s), and hence the sheet resistance of the p^+-type well 86 must be set to 300 k Ω/□ or less.

Page 141, paragraph beginning at line 11, please delete in its entirety and insert therefor the following new paragraph:

It is sufficient for the amplification transistor 2 of the unit cell to drive the vertical signal line 8 and the gate of the slice transistor 150. Since the gate capacitance of the gate of the slice transistor 150 is much smaller than the clamp capacitor as in the conventional device, it is possible to shorten the time required for suppressing noise. Therefore, it is possible to surely suppress noise during a horizontal blanking period in a case of a television signal processing.

Page 142, paragraph beginning at line 5, please delete in its entirety and insert

therefor the following new paragraph:

Note that the second slice pulse 109 may be influenced by the immediately preceding first slice pulse 107. The operations of the first and second slice pulses 107 and 109 can be effectively equalized by inserting a dummy slice pulse immediately before the first slice pulse 107. The operations mean that whether or not preceding pulse is included. In this case, in order to equalize the operation of the first pulse with that of the second pulse which has a preceding pulse, a dummy pulse is added preceding to the first pulse.

Page 143, paragraph beginning at line 21, please delete in its entirety and insert therefor the following new paragraph:

$$P8 < P11 < P12 < P3 < P4;$$ and preferably

Page 145, paragraph beginning at line 6, please delete in its entirety and insert therefor the following new paragraph:

According to the present embodiment, an amplifying type MOS sensor has a noise canceler, between an edge of the vertical signal line and the horizontal selection transistor, for suppressing the noise by converting a voltage appeared at the vertical signal line into a charge and performing a subtraction processing in a charge domain. Therefore, the noise due to the threshold variation of the amplification transistors can be suppressed in a short period of time. It is possible to surely suppress noise during a horizontal blanking period in a case of a television signal processing.

Page 146, paragraph beginning at line 2, please delete in its entirety and insert therefor the following new paragraph:

According to the present embodiment, there can be provided a solid-state imaging device in which the noise due to the threshold variation of the amplification transistors can be suppressed in a short period of time and it is possible to surely suppress noise during a horizontal blanking period in a case of a television signal processing.

Page 147, paragraph beginning at line 22, please delete in its entirety and insert therefor the following new paragraph:

The present invention is characterized in that the clamp capacitor and the sample/hold capacitor are formed in the same area on the semiconductor substrate in a partially or completely overlapping manner. It may be desirable to set the reset drain power source voltage substantially equal to the video bias voltage.

Page 149, paragraph beginning at line 17, please delete in its entirety and insert therefor the following new paragraph:

Gate voltages of the amplification transistors 2-1-1, 2-1-2, ..., 2-1-n, i.e., substantially same voltages of the photodiode voltages appear on the vertical signal lines 8-1, 8-2, ..., 8-n. A clamp pulse 102 is applied to the gates of the clamp transistors 40(40-1, 40-2, ..., 40-n) to turn on the clamp transistors 40(40-1, 40-2, ..., 40-n). The clamp nodes 36(36-1, 36-2, ..., 36-n) are fixed to the same voltage as a clamp power source 38.

Page 149, paragraph beginning at line 26, please delete in its entirety and insert therefor the following new paragraph:

After the clamp transistors 40(40-1, 40-2, ..., 40-n) are turned off, a reset pulse 103 is generated from the vertical address circuit 5 to make the reset line 7-1 high and is applied to the reset line 7-1. The reset transistors 4(4-1-1, 4-1-2, ..., 4-1-n) of the unit cells P1-1-1, P1-1-2, ..., P1-1-n arrayed in the first row which are connected to the reset line 7-1 are turned on to reset the signal charge. A sum of voltages obtained by dividing differential voltages between the voltages set when the signal charges are present at the photodiodes 1-1-1, 1-1-2, ..., 1-1-n and the voltages set when the signal charges are not present with a ratio between the clamp capacitor 32 and the sample/hold capacitor 34 and the voltage of the clamp power source 38 appear on the clamp nodes 36-1, 36-2, ..., 36-n.

Page 150, paragraph beginning at line 26, please delete in its entirety and insert

therefor the following new paragraph:

Horizontal selection pulses 105(105-1, ..., 105-3) are sequentially supplied to the horizontal selection transistors 12-1, 12-2, ..., 12-n from the horizontal address circuit 14 to sequentially output signal of one line. By sequentially performing this operation for the subsequent lines, all the signals in the two-dimensional matrix arrayed unit cells can be read out.

Page 154, paragraph beginning at line 1, please delete in its entirety and insert therefor the following new paragraph:

A construction of FIG. 52 will be described for the purpose of reducing a fixed pattern noise. In FIG. 52, unit cells comprising amplifying transistor 2 (2-1-1, 2-1-2, ..., 2-3-3) for selecting a line which reads out a signal of photodiodes 1 (1-1-1, 1-1-2, ..., 1-3-3), vertical selection transistors 3 (3-1-1, 3-1-2, ..., 3-3-3) for selecting a line which reads out a signal and reset transistors 4 (4-1-1, 4-1-2, ..., 4-3-3) for resetting a signal electric charge, are arranged in a two-dimensional 3 x 3 matrix. Of course, a larger number of unit cells are arranged in the actual apparatus.

Page 161, paragraph beginning at line 20, please delete in its entirety and insert therefor the following new paragraph:

FIG. 55 shows a variation of the vertical signal line potential and the clamp node potential with time elapse. In the present embodiment, when a potential in which the vertical signal line potential returns at the time of clamping and a potential in which the vertical signal line potential returns at the time of sample/hold are the same, as in a dark time when the signal is zero, the potential of the clamp node when the sample/hold is completed does not return to a, value which is approximate to the ΔV_{CL} and becomes zero. Therefore, there is no inconvenience such as a signal corresponding to ΔV_{CL} being generated even if it is a dark time and the signal is zero. Therefore, it is possible to prevent the noise due to the

variation in ΔV_{CL} from being generated.

Page 165, paragraph beginning at line 2, please delete in its entirety and insert therefor the following new paragraph:

If a magnitude of the correction capacitor C_{CMP} is set in a range of $2\{C_{CL} - C_{CL} \cdot C_{SH}/(C_{CL} + C_{SH})\} > C_{CMP} > 0$, the capacitor C approaches the magnitude of C_{CL} as compared with a case in which the correction capacitor does not exist. Therefore, the difference V_{CL} becomes smaller and thus, the noise also becomes smaller.

Page 173, paragraph beginning at line 3, please delete in its entirety and insert therefor the following new paragraph:

In general, in the amplification-type MOS-type solid-state imaging device, an output signal of the photodiode which is a light receiving portion corresponding to the pixel in each of the unit cells is amplified and taken out through the amplification transistor 64 provided in the unit cell. Therefore, at the time of such amplification, a variation in threshold voltage of the amplification transistor 64 is added to the signal. Therefore, even if the potentials of the photodiodes 62 of the unit cells are the same, the amplification transistor is different depending on unit cell to which the photodiode belongs, and the threshold voltages of the amplification transistors 64 are different from each other. Therefore, the output signals are not the same, and if an image is reproduced, noise is generated in corresponding to a variation in threshold value of the amplification transistor 64.

Page 174, paragraph beginning at line 13, please delete in its entirety and insert therefor the following new paragraph:

As described above, the threshold voltages of the amplification transistors 64 in the unit cells are different, and each of the threshold voltage is particular or unique depending on the unit cell. Therefore, there is generated noise which is locally fixed and distributed to the reproduced image, i.e., two-dimensional noise. As previously described, such noise is called

fixed-pattern noise because the noise is locally fixed on a screen which is a two-dimensional space.

Page 174, paragraph beginning at line 23, please delete in its entirety and insert therefor the following new paragraph:

Therefore, in the present embodiment, there is provided a noise reduction circuit (noise canceler circuit) for suppressing the fixed-pattern noises, instead of a circuit comprising the signal transmitting transistor and the accumulation capacitor of the output portion in the circuit shown in FIG. 1 which shows the conventional structure. Although FIG. 57 shows a correlation double sampling type noise reduction circuit (noise canceler circuit) in which a difference between a signal and a noise in an voltage region, the type of the noise reduction circuit is not limited to the correlation double sampling type, and various noise reduction circuit may be used.

Page 186, paragraph beginning at line 18, please delete in its entirety and insert therefor the following new paragraph:

Furthermore, in the present embodiment, the unit cell is provided therein with two photodiodes which constitute light receiving portions, and the two photodiodes commonly include one set of output circuits. Therefore, when the MOS-type solid-state imaging device of the present embodiment is applied for imaging of a television, the number of reading out an electric charge signal using the amplification transistor 64 during one horizontal blanking period is one and thus, it is easy to drive the drive. In short, the feature of the present embodiment is that a direction of reading out and a direction of commonly possession are different from each other.

Page 195, paragraph beginning at line 3, please delete in its entirety and insert therefor the following new paragraph:

In the case of the television scheme, a horizontal blanking interval is provided, and an

image signal is not sent during this interval. Therefore, it is necessary to suppress, to a certain level, the disturbances in the potential of the p-type well 86 due to the above-mentioned reset pulse. Accordingly, in the NTSC scheme, which is the existing television scheme, the noise reduction circuit (noise canceler circuit) is operated in an interval of about 11 (μs), which is a horizontal blanking interval. Disturbances in the potential of the p-type well 86 must be suppressed to about 0.1 (mV) within this interval.

Page 195, paragraph beginning at line 15, please delete in its entirety and insert therefor the following new paragraph:

Such a small value as 0.1 (mV) is set because the noise voltage output of the CCD corresponds to this. According to a detailed analysis, to settle the disturbances to a value as small as 0.1 (mV) within the very short time interval of 11 (μs), the sheet resistance of the p-type well 86 must be set to 1 k Ω/□ or less. This is about 1/100 the sheet resistance of the conventional CCD.

Page 195, paragraph beginning at line 23, please delete in its entirety and insert therefor the following new paragraph:

For this purpose, the impurity concentration of the p-type well 86 must be increased to about 100 times. Such a concentration can not be set in the CCD, as described above with reference to the p-type substrate. Furthermore, in the high-vision television scheme, the horizontal blanking interval is 3.77 (μs), and hence the sheet resistance of the p-type well 86 must be set to 300 k Ω/□ or less.

Page 198, paragraph beginning at line 27, please delete in its entirety and insert therefor the following new paragraph:

In addition, since an output from each unit cell is output through the noise canceler circuit, fixed pattern noise due to threshold variations of the amplification transistor of each unit cell can be removed. In the present embodiment, an output of the unit cell is output

through the noise canceler circuit of the present invention which is capable of operating at high speed. Therefore, even if the MOS sensor is applied to an animation imaging device, it is possible to remove the fixed-pattern noise due to the threshold variations of the amplification transistor of the unit cell within every frame of within a time period limited for every frame. Therefore, it is possible to provide an amplification-type MOS solid-state imaging device which is sufficiently utilized even for the television scheme. Further, in the noise canceler circuit, the clamp capacitor 32-1, 32-2, ... (simply referred to 32, the same is applied to other reference numerals having appendixes) and the sample/hold capacitor 34 are directly and closely connected to each other so that they can be stacked on the same portion. Therefore, the capacitors can be small in size.

A35 Cont'd

Page 206, paragraph beginning at line 27, please delete in its entirety and insert therefor the following new paragraph:

In the noise canceler circuit of twenty-sixth embodiment, even if an accuracy of the noise cancel is not sufficient, it is possible to provide a noise canceler circuit which is capable of canceling noise with high accuracy, by providing the impedance conversion circuit of twenty-fifth embodiment, thereby impedance-converting an output of a unit cell, so as to substantially equalize the impedance of the noise canceler circuit as viewed from the unit cell at the time of outputting only noise component and at the time of outputting signal component and noise component, so that the noise components of both the cases become substantially the same.

A36

Page 209, paragraph beginning at line 1, please delete in its entirety and insert therefor the following new paragraph:

The slice transistors 150-1, 150-2, ... are connected at their ends near the drain to the signal output terminal (horizontal signal line) 15 through source-drain of the corresponding horizontal (row) selection transistors 12-1, 12-2, . . . , respectively. The horizontal selection

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transistors 12-1, 12-2, ... are driven by horizontal address pulses supplied from the horizontal address circuit 13.

Page 209, paragraph beginning at line 9, please delete in its entirety and insert therefor the following new paragraph:

In order to reset the source potentials of the slice transistors 150-1, 150-2, ..., the slice reset transistors 156-1, 156-2, ... are provided between the sources of the slice transistors 150-1, 150-2, ... and the slice electric power source terminal 158. A slice reset terminal 160 is connected to gates of the transistors 156-1, 156-2, . . . That is, the source sides of the slice transistors 150-1, 150-2, ... are connected to the slice electric power source terminal 158 through source drains of the corresponding transistors 156-1, 156-2, ..., respectively. The gate sides of the slice reset transistors 156-1, 156-2, are connected to the slice reset terminal 160. The slice reset transistors 156-1, 156-2, ... are turned on at the timing of the slice reset pulse supplied from the slice reset terminal 160, and the source potentials of the slice transistors 150-1, 150-2, ... are reset.

Page 210, paragraph beginning at line 18, please delete in its entirety and insert therefor the following new paragraph:

In this manner, the noise canceler circuit of the MOS sensor of twenty-eighth embodiment is characterized in that voltages appearing on the vertical signal lines 8-1, 8-2, ... are converted to electric charges through gate capacitors of the slice transistors 150-1, 150-2, ..., and a subtraction is performed in the electric charge region, thereby suppressing the noise. The noise canceler circuit having a system in which the noise are canceled in the electric charge region is connected to the unit cell P1-i-j which is the same as that of the twenty-seventh embodiment, thereby constituting a solid-state imaging device.

Page 211, paragraph beginning at line 22, please delete in its entirety and insert therefor the following new paragraph:

When the slice reset pulse of the slice reset terminal 160 disappears, the slice reset transistors 156-1, 156-2, ... are turned off, and the slice capacitors 152-1, 152-2, ... are brought into a state where they can be electrically charged. Then, a first slice pulse SP1 is applied to the slice pulse supply terminal 154.

Page 217, paragraph beginning at line 5, please delete in its entirety and insert therefor the following new paragraph:

As described above, according to twenty-eighth embodiment, because an output of the unit cell is output through the noise canceler circuit, it is possible to eliminate fixed-pattern noise corresponding to the threshold variations of the amplification transistor of the unit cell.

Page 217, paragraph beginning at line 11, please delete in its entirety and insert therefor the following new paragraph:

In the present embodiment, an output from the unit cell is supplied to the noise canceler circuit through the gate capacitor of the slice transistor. Therefore, even if the noise component is output or the signal component and noise component is output, the impedance of the noise canceler circuit as viewed from the unit cell is substantially the same. For this reason, the noise components of both the cases are substantially the same, and if the subtraction of the two outputs is performed, the noise output can be exactly canceled so that only the signal component can be output.

Page 218, paragraph beginning at line 9, please delete in its entirety and insert therefor the following new paragraph:

If amplitudes of the first and second slice pulses are the same, a signal electric charge may not be read out in an extremely small signal region, or a linearity may be deteriorated. In this case, it is effective to stabilize the operation to make the amplitude of the second slice pulse greater than that of the first slice pulse, thereby adding a bias electric charge to an

electric charge which is read out by the second slice pulse. Further, it is also effective to make a width of the second slice pulse wider than that of the first slice pulse.

Page 221, paragraph beginning at line 10, please delete in its entirety and insert therefor the following new paragraph:

Therefore, if a size of the correction capacitor C_{CMP} is set in a range of $2\{C_{CL} - C_{CL} \cdot C_{SH} (C_{CL} + C_{SH})\} > C_{CMP} > 0$, the capacity connected to the vertical signal line at the time of sample/hold approaches a size of the capacity C_{CL} of the clamp capacitors 131-1, 131-2, ... Therefore, a difference VCL in voltage generated due to this difference in capacity becomes smaller and thus, noise is also reduced.

Page 222, paragraph beginning at line 12, please delete in its entirety and insert therefor the following new paragraph:

According to the present embodiment, as described above, in the MOS-type solid-state imaging element having a noise eliminating circuit, it is possible to suppress the variations in capacity during the noise eliminating operation which is the causes for generating noise, by providing the vertical signal line 8 with the correction capacitors 160-1, 160-2, ..., which contributes to reduce the noise. That is, the impedances as viewed from the cell becomes the same between a case where signal component and noise component is output and a case where noise component is output, and noise can accurately be canceled. In this case, it should be noted that noise component is output, when the reset operation is completed, and signal component and noise component is output after PD (photodiode) is selected.

Page 223, paragraph beginning at line 25, please delete in its entirety and insert therefor the following new paragraph:

The thirty-first embodiment has unit cells whose structures are different from those in twenty-sixth to thirtieth embodiments. The entire structure is the same as that in twenty-fifth

embodiment shown in FIG. 57 and thus, the entire structure is not illustrated here. Thirtieth-first embodiment is characterized in that a unit cell P2 shown in FIG. 77 is used instead of the unit cell P1 in FIG. 57.

Page 228, paragraph beginning at line 18, please delete in its entirety and insert therefor the following new paragraph:

Further, the present is not limited to the above described embodiments, and various modifications may be made. For example, if the amplification transistor of the unit cell can be manufactured so that the threshold value is not varied, a fixed-pattern noise is not generated and therefore, the noise canceler circuit can be omitted. Even if the fixed-pattern noise is generated, if there is no influence on picture quality, the noise canceler circuit can likewise be omitted.

Page 229, paragraph beginning at line 6, please delete in its entirety and insert therefor the following new paragraph:

In the noise canceler circuit in each of the embodiments, when a signal electric current (noise component only) which is read out when there is no input signal is small, noise are lower. Therefore it is preferable to substantially equalize a voltage applied to the accumulation drain electric power source terminal and a video bias voltage. The video bias voltage is a voltage at which the signal output terminal 15 is substantially fixed when a signal is read out in the form of electric current from the signal output terminal 15. Such a modification is shown in FIG. 45. An operational amplifier 176 is connected to the signal output terminal 15, and a load resistance 178 is connected between input and output end portions of the operational amplifier 176. With this arrangement, a signal electric current is forcibly flowed to the load resistance 178, and the horizontal signal line 15 is fixed to an imaginary certain voltage, i.e., a video bias voltage.

Page 230, paragraph beginning at line 6, please delete in its entirety and insert

therefor the following new paragraph:

Various examples which can obtain picture signals free from noise by combining the amplification-type MOS-type sensor and the noise canceler have been described above.

Page 231, paragraph beginning at line 19, please delete in its entirety and insert therefor the following new paragraph:

A basic cell P8-i-j of the present embodiment comprises a photodiode 62-i-j for detecting an incident light, an amplification transistor 64-i-j having a gate to which a cathode of the photodiode 62-i-j is connected for amplifying the detection signal therefrom, a reset transistor 66-i-j to which the cathode of the photodiode 62-i-j (the gate of the amplification transistor 64-i-j) is connected for resetting a signal electric charge, and an address capacitor 69-i-j connected between a drain and the gate of the amplification transistor 64-i-j. In the present embodiment, the vertical selection transistor 3-i-j provided in the conventional device (FIG. 1) is omitted, and the address capacitor 69-i-j is newly added.

Page 236, paragraph beginning at line 2, please delete in its entirety and insert therefor the following new paragraph:

In generally, in the amplification-type MOS-type solid-state imaging device, because variations of threshold voltage of the amplification transistor 64 is superposed on a signal, even if a potential of the photodiode 62 is the same, an output signal may vary. Therefore, if a photographed picture is reproduced, two-dimensional noise (which means that noise are locally fixed, and this is called fixed-pattern noise) corresponding to threshold variations of the amplification transistor 64 is generated. However, according to the present embodiment, as described above, a voltage corresponding to a difference between a case where there is a signal electric charge in the unit cell and a case where the signal is reset and there is no signal electric charge finally appears on the clamp nodes 145-1, 145-2, .., and therefore, a fixed-pattern noises due to threshold variation of the amplification transistor 64 is suppressed. That

is, the circuit comprising the clamp capacitor 131, the clamp transistor 132, the sample/hold transistor 133 and the sample/hold capacitor 134 serves as a noise canceler.

Page 241, paragraph beginning at line 9, please delete in its entirety and insert therefor the following new paragraph:

In the NTSC scheme, which is the existing television scheme, the noise reduction circuit is operated in an interval of about 11 (μs), which is a horizontal blanking interval. Disturbances in the potential of the p-type well 86 must be suppressed to about 0.1 (mV) within this interval.

Page 241, paragraph beginning at line 15, please delete in its entirety and insert therefor the following new paragraph:

Such a small value as 0.1 (mV) is set because the noise voltage output of the CCD corresponds to this. According to a detailed analysis, to settle the disturbances to a value as small as 0.1 (mV) within the very short time interval of 11 (μs), the sheet resistance of the p^+-type well 86 must be set to 1 k Ω/□ or less. This is about 1/100 the sheet resistance of the conventional CCD.

Page 241, paragraph beginning at line 23, please delete in its entirety and insert therefor the following new paragraph:

For this purpose, the impurity concentration of the p^+-type well 86 must be increased to about 100 times. Such a concentration can not be set in the CCD, as described above with reference to the p-type substrate. Furthermore, in the high-vision television scheme, the horizontal blanking interval is 3.77 (μs), and hence the sheet resistance of the p^+-type well 86 must be set to 300 k Ω/□ or less.

Page 244, paragraph beginning at line 14, please delete in its entirety and insert therefor the following new paragraph:

Further, because an output of the unit cell is output through the noise canceler, it is

possible to suppress the fixed-pattern noise corresponding to the threshold variations of the amplification transistor of the unit cell.

Page 244, paragraph beginning at line 19, please delete in its entirety and insert therefor the following new paragraph:

Further, if a substrate comprising a p^--type impurity substrate and a p^+-type impurity substrate formed on the p^--type impurity substrate is used as a semiconductor substrate forming the unit cell, it is possible to reduce the dark current following into the unit cell, and to stabilize a potential on a surface of the substrate. Therefore, it is possible to reliably operate the noise canceler circuit.

Page 248, paragraph beginning at line 16, please delete in its entirety and insert therefor the following new paragraph:

Then, the common gate 37 of the sample/hold transistors 30-1, 30-2, ... is brought into low level to turn off the sample/hold transistors 30-1, 30-2, ... With this operation, voltages free from noise appearing on the clamp nodes 41-1, 41-2, ... are accumulated in the sample/hold capacitors 34-1, ...

Page 251, paragraph beginning at line 2, please delete in its entirety and insert therefor the following new paragraph:

That is, impedances of the noise canceler circuit as viewed from the unit cell are substantially the same between a case where the noise component is output and a case where the signal component and noise component are output. Therefore, the noise components of both the cases are substantially the same, and if a difference in noise component between both the cases is eliminated, it is possible to accurately eliminate the noise output and to output only the, signal component. Therefore, it is possible to accurately cancel the noise [noises]. Further, if the noise canceler circuit is viewed from the unit cell, only the gate capacitor can be seen in view of impedance, and its volume is extremely small. Therefore, it

is possible to reliably cancel the noise in a short period of time.

Page 254, paragraph beginning at line 5, please delete in its entirety and insert therefor the following new paragraph:

The MOS sensor of thirty-seventh embodiment has the same structure of the unit cell P8-i-j as that in thirty-third embodiment shown in FIG. 81, but has a different structure of the noise canceler. The noise canceler of thirty-seventh embodiment converts a voltage appearing on the vertical signal lines 8-1, 8-2, ... into gate capacitor of the slice transistor 150, and performs a subtraction in an electric charge region, thereby suppressing the noise.

Page 257, paragraph beginning at line 19, please delete in its entirety and insert therefor the following new paragraph:

As described above, according to thirty-seventh embodiment, because an output of the unit cell is output through the noise canceler, it is possible to eliminate fixed-pattern noise corresponding to the threshold variations of the amplification transistor of the unit cell.

Page 261, paragraph beginning at line 6, please delete in its entirety and insert therefor the following new paragraph:

FIG. 55 shows a variation with time elapse of a potential of the vertical signal line 8 and a potential of the clamp node 145. In the present embodiment, as in a dark time case in which the signal is zero, even if potentials of the vertical signal line 8 in which the potential returns at the time of clamping and the potential returns at the time of sample/hold are the same, the potential of the clamp node, when the sample/hold is completed does not return to a value which is approximate to ΔV_{CL} and becomes zero. Therefore, there causes no inconvenience that even though it is a dark time in which the signal is zero, a signal corresponding to ΔV_{CL} may appear. Therefore, it is possible to prevent noise due to variation of ΔV_{CL} from being generated.